Tutorial Programme Monday June 15th

AM	1 Changing Role of Packaging from Packaging of ICs to Packaging of Systems with High Impact Rao Tummala Georgia Tech	2 Physical and Electrical Design Modelling Prof Flavio Canavero Turin Polytechnic	3 Electronic Package Reliability N Sinnadurai	7 Wirebonding Technologies Seminar Part I H&K ESEC K&S ASM F K Delvotec Palomar Hereaus
PM	5 TSV Technology for 3D Integration Latest developments EMC3D consortium	6 Advanced materials for power electronics packaging Dr.-Ing Schulz-Harder Mark A. Occhionero, Ph.D. Dr. Ing. Roberto Bellu	4 Mems and Sensors Applications Ciprian Iliescu A Star Singapore	7 Wirebonding Seminar part II

TU1
EMERGING NEED AND TREND FROM 3D ICs TO 3D SYSTEMS

Prof .Rao Tummala and Ritwik Chatterjee – Microsystems Packaging Research Center(PRC)
Georgia Tech.

Course Objectives:

This course presents an overview of emerging need and trends from 3D ICs to 3D Systems,for highly integrated and microminiaturized convergent systems for consumer, computer, automotive, aerospace, communication and bio-medical applications.

The first electronics wave, which started with the invention of the transistor, has been largely due to Moore's Law and the associated hybrid and discrete component-based approaches to systems using 100's of discrete components made of ceramics, organics, metals, solders and alloys. The end of this CMOS-based era using this traditional approach seems evident beyond 32 nm. This is primarily due to the lack of lithographic-driven electrical performance improvement, unlike in the past. So the obvious question is how to achieve the improved performance.

One approach is to pursue alternative devices to CMOS. The second alternative is to pursue 3D ICs,but 3D ICs constitute a small part of the system.A better and more complete altrernative to systems appears to be 3D systems presented in this course , the focus of which is on system integration, miniaturization, functionality and cost, rather than or in addition to device-based CMOS wafer fabs beyond 32 nm and the resulting 3D ICs. This focus should allow improved systems functionality without massive wafer fab investments. The R&D and manufacturing investments, however, are necessary in system wafer fabs. This is the rationale for this course.

This course reviews the progress and challenges in SOC. It also reviews the progress in 3D ICs by stacking of ICs and packages enabled by recent progress in TSV. It describes the remaining challenges in applying these technologies for cost effective products. It goes beyond these 3D technologies and introduces the concept of 3D Systems and the concept of system-on-panel(SOP) , in contrast to device wafer, to date. In this approach, the electronics system functionality and performance are achieved by system miniaturization by means of micro and nano-materials, structures, components and 3D interconnections as well miniaturized batteries and thermal materials and interfaces.

Tu2
"Physical and Electrical Design Modelling"

Prof Flavio G. Canavero Politecnico di Torino, Italy

The growth of high-speed and high-performance information and communication devices introduces new challenges during the electrical design and rapid prototyping phases of these systems. New modelling methodologies and associated CAD tools are already available to facilitate the mixed-signal electrical design of such highly compact and complex packages. This tutorial presents an overview of modelling and simulation strategies with emphasis on algorithms and applications of model-order reduction techniques.

Tu3
Electronics Reliability Tutorial

Nihal Sinnadurai

CONTENTS

PART 1. GENERIC RELIABILITY

- Quality and Reliability –quality and its benefits, reliability regimes, and how quality benefits reliability.
- Life Cycle Reliability – the Bathtub curve and Reliability Regimes
- Infant mortalities and burn-in at the component level
  - improving burn-in throughput
  - burn-in and ESD hazards
- Infant mortalities and environmental stress screening (ESS) at the board level
  - benefits of ESS over constant temperature burn-in.
  - Causes of board level latent faults – Designing and Engineering for Reliability
- Random Failures and their causes
  - determining Random Failures, are the handbooks of any use in Designing for Reliability?
  - benefits from best practice manufacturing
  - Process Engineering for Reliability
- Wearout Failures and their causes
  - failure mechanisms – influences from design, technology, environment
  - modelling failure mechanisms and Designing for Reliability.
  - accelerated ageing, by thermal overstress, damp heat overstress, cyclic stresses

PART 2. CASE STUDIES OF ELECTRONICS

- Case Studies Towards Designing And Building For Reliability
  - Integrated circuit mechanisms
  - Passivations
  - Metallisations
  - Wire Bonds
- Packaging Reliability
  - Encapsulation
  - Popcorn Avoidance and Yield Improvement
- Active circuit reliability
- PCB wearout mechanisms

Electrical Package reliability

Tu4
Recent trends in MEMS and BioMEMS packaging

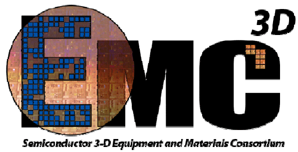
Ciprian Iliescu, Bangtao Chen, Guolin Xu, Jiashen Wei

Institute of Bioengineering and Nanotechnology, 31 Biopolis Way, The Nanos, Singapore 138669

The Tutorial will be focus on the recent trends in MEMS/BioMEMS packaging technologies and will provide a broad overview of the novel and significant developments, both as a means to introduce newcomers and to update the more experienced with the latest and cutting edge advances in this field.

It is recognize that a major part of the MEMS device fabrication cost is in packaging and testing. For this reason a special attention will be given to wafer level packaging (WLP) methods of MEMS devices. In general terms, the method consist in encapsulation of the sensitive part of the MEMS device, at wafer level, between two other wafers (silicon or glass) using bonding techniques. One of these wafers presents holes for electrical feedtrough. Various WLP solutions using interfacial bonding (such as anodic bonding, metal bonding or plasma activated bonding), boding using intermediate melting materials (such as low melting temperature glass and solder) or adhesive bonding (using BCB, parylene or SU8) are presented. Electrical feedtrough is needed for interconnection between the active part of the MEMS device and PCB: lateral and vertical feedthrough techniques will be described. Surface micromachining can be used in packaging at wafer level. In this technique, a sacrificial layer is usually etched through a porous membrane and finally a metal is deposited on the membrane for hermetical sealing. Examples of classical MEMS devices (such as: pressure sensors, accelerometers, gyroscopes, microphone etc) packaged at wafer level are also analyzed.

MEMS application in biology (so-called BioMEMS) becomes a very “hot” field due to the benefit of miniaturization with a main effect on the fabrication costs. A first problem for BioMEMS devices is the biocompatibility of the material in contact with the biological sample. “Biocompatibility of MEMS materials” will be one of subject to be discussed. Problems related packaging of implantable bioMEMS devices, as well as biosensors and lab on chip devices are also presented. Finally examples of microfluidic devices, fabricated in glass and packaged at wafer level are shown.



Tu5
Latest Advancements in TSV Technology for 3D Integration

Symposium Agenda

13:00 - 13:30 EMC3D Activities for 3D Integration
Semitool

13:30 - 14:00 Precision Bonding Techniques for Homogeneous and Heterogeneous TSV Stacking
EV Group

14:00 – 14:30 Solutions to Cost Effective Via Etching
Applied Materials

14:30 – 15:00 Insulator/Barrier and Seed Metallization
Applied Materials

15:00 – 15:30 Advanced TSV Metallization
Semitool

15:30 – 16:00 Break Time

16:00 – 16:30 New Materials / Processes for 3D Integration
Rohm and Haas Electronic Materials

16:30 – 16:45 Dielectric Films, CMP and Integration
Applied Materials

16:45 – 17:10 Pick and Place for Chip Stacking
Datacon Technology GmbH

17:10 – 17:35 Thinned Wafer Handling Materials Development
Brewer Science

17:35 – 18:00 TSV Challenges in Process and Integration
Texas A&M

18:00 – 18:30 Current and Future 3D Activities
LETI

Tu6

Advanced materials for High Power Electronics packaging

Dr.-Ing Schulz-Harder Technical Director Electrovac Curamik GmbH
Mark A. Occhionero, Ph.D. Senior Research Scientist / VP of Marketing and Technical Sales CPS Technologies Corporation USA
Dr. Ing. Roberto Bellu Consultant Engineer

1. **High reliability demand in high power applications**
   Outline of semiconductor device reliability
   Examples:
   - Automotive and similar
     - Construction principles of Power Modules and their reliability limit
     - Automotive environment and lifetime requirement
     - Power module design for Automotive requirements
   - Converters for wind power
     - Lower losses
     - High efficiency
     - Modular construction
     - High reliability with lowest costs
   - Lift/escalators
   - Medical/life-support applications
   - Defense applications
     - Light weight
     - Small dimensions
     - Ruggedness

2. **Failure mechanisms: statistical approach on main causes of failure**
   Mechanical, electrical point of view
   Examples:
   - Thermal shocks
   - Thermal fatigue
   - Mechanical shocks
   - Vibration

3. **Technological answers: the role of advanced materials**
   Exploit characteristics of advanced materials
   Examples:
   - Advanced ceramics
     - Substrates having excellent electric isolation, low thermal resistance and silicon matched CTE
     - DBC Direct Bonded Copper Substrates;
     - Reliability requirements for ambient and thermal cycling conditions exceeding those of industrial applications
     - Critical areas in High Power modules assembly
     - Liquid cooling of High Power electronics
   - Composite materials
     - Ideal material properties considered for ideal for “thermal management”
     - Review of materials available comparison of properties
     - Review of AlSiC properties – Ideal application for high power electronics thermal management
     - Production process review
       - Discussion of process steps AlSiC general and process comparisons

    - Discussion of CPS process steps
    - Discussion for functional shape capability

- Discussion on IGBT application
    - Case study on application
- Discussion HEV applications
    - Functional shapes – and fabrication
    - Cost effective design and design for manufacturability
- Discussion of microprocessor lid applications
    - Case study on application
    - AlSiC properties beyond thermal management that improve thermal dissipation

4. Emerging applications: modules for concentrated photovoltaic

- Need for reliability
- Need for performances

5. Practical approach

- Understand what we really need
- Trade off: cost-performances
- From modelling and simulation to design and prototyping
- Always keep in mind ease of manufacturing when speaking of quality and reliability.

TU7
Wirebonding Seminar

9:00 ESEC D Lek The materials science of wirebonding
10:00 Dott. Hesse Hesse and Knipps Integrated bond quality monitoring
10:30 break
11:00 K&S B Chylak CU wirebonding
12:00Lunch

1:30 Palomar D Evans Chain Wire Bonding of a RF-SOE package using a Gold Ball BonderFK Delvotec
2:00 ASM C Vath Factors Affecting The Long Term Stability Of 20 Micron Copper Wire Bonded To Aluminum Bonding Pads
3:00 break
3:30 FK Delvotec Dr. Sedlmair Perfection through Inspection:The way to Zero defect Producttion of Wire bonds
4:00 Hereaus AL ribbon bonding, overview, state of the art application and outlook

The Materials Science of Ballbonding: A Brief Overview

Dr. Christopher D Breach, Esec

Thermosonic ballbonding is a metallurgical process that until recently was rarely the subject of metallurgical analysis. However, in recent years greater focus has been given to the materials science of thermosonic ball – wedge bonding in an attempt to better control and advance its application as an interconnect technology in advanced packaging. As with most materials processes, establishing a scientific understanding of the process requires knowledge from various sub-disciplines of physical science. This presentation briefly reviews the current understanding of the materials science of ballbonding including free air ball deformation and ball bond formation, wire properties and 2nd bond formation and intermetallic growth.

Chain Wire Bonding of a RF-SOE package using a Gold Ball Bonder

D Evans Palomar

RF-SOE power transistors are traditionally wire bonded using gold wedge bonders to create strings of loop profiles with short and long wires.
A ball bond technology (chain bonding) to create a ball-loop-stitch-loop-stitch-loop-stitch … is demonstrated as alternative to these traditionally wedge bond solutions.
Initial chain bonding results using a ball bonder produced comparable performance as a wedge bonded product, but using more prevalent ball bonding technology.
This paper will introduced the reader to the RF-SOE package wire bonding requirements then actual results achieved using chain bonding technology.

Recent developments to enable fine pitch
Copper wire bonding production

Kulicke and Soffa Ind. Inc
Bob Chylak
Vice President Packaging and Process Integration

Copper wire bonding has huge cost advantages over gold wire bonding. Low pin count heavy wire applications have already been converted to copper wire and many companies are in high volume production. There has also been an extensive amount of development activity that has targeted high pin count (>200 I/O) and high performance applications. Recently we have seen a dramatic shift in this direction. Companies have made the switch for these high I/O fine wire packages to copper wire bonding in production in much faster and in larger quantities then were earlier predicted.

Developments in Wire bonder technology, and materials have enabled this transition. While converting to a copper wire bonding process needs to be done carefully, recent technology developments have greatly improved the rate of success. Wire Bonding and materials companies have invested heavily in R&D and are starting to see the fruits of their labor. In this presentation I will discuss some the technology developments that have overcome the challenges and make recommendations for implementing Copper wire bonding as a replacement for Gold in high volume manufacturing of high pin count packages.

Specific areas of technology development that will be covered are controlling pad damage, second bond optimization, looping with copper wire, molding considerations, and achieving reliability targets. The focus is on understanding potential issues and optimizing the copper process on these types of applications for a stable and robust production process.

Perfection through Inspection:
The Way to Zero-Defect Production of Wire Bonds

FK Delvotec Dr. Sedlmair

Zero-Defect Production is becoming a key strategy in electronics manufacturing because of higher product quality and a number of corollary advantages such as better overall process control and sharply reduced manufacturing complexity.

Automatic Optical Inspection systems are widely used to achieve 100% inspection of production volume. Their standard working principle is comparing the image of an ideal part to the part under inspection and accepting or rejecting it if the image correspondence is below a certain, definable threshold. Overall these systems operate very similar to classical visual inspection.

The real strength of automatic inspection systems can, however, be exploited only when images are not just compared but quantitatively evaluated. In this fashion, numerical parameters of interest to the wire bonding engineer can be extracted from wire bond pictures, such as the position of the bond foot on the bond pad; the width, length, deformation and symmetry of the bond foot; loop length, loop shape and even loop height. With numerical values in hand, they can be compared against pre-set thresholds and used to reject defective parts.

Even more interesting is the capacity to run a full SPC. In this way the actual mean values and standard deviations, i.e. the process capability, is accessible in a very simple and economic fashion for 100% of production volume without any penalty in throughput because the inspection systems can run fully parallel to the wire bonder. This permits spotting any adverse trends and counteracting long before a defect occurs.

F&K Delvotec has developed a PBI (post-bond inspection) system which is specifically designed for die-bonding and wire-bonding. Its scope and possible utilization is discussed in detail in this paper, as are several further potential developments from this approach.

Factors Affecting The Long Term Stability Of 20 Micron Copper Wire
Bonded To Aluminum Bonding Pads

Charles J. Vath, III, Gunasekaran A/L Muthusamy
ASM Technology Singapore Pte. Ltd.

This paper will present the findings of work performed on 20 micron diameter copper wire of three different wire purities from two suppliers. The wires were analyzed for their composition and all materials used in building the samples were analyzed for their halogen content using ICP AES, ICP MS, or similar techniques. The test die was mounted on BT resin substrates. The bonding parameters were optimized for each wire used. Part of the optimization process involved monitoring the flatness of the bonded ball and the amount of aluminum remaining under the bond. The crystal structure of the wire, the free air ball, and the bonded ball were examined using EBSD and OIM techniques. The hardness of the material for each configuration was also measured and correlated with the EBSD and OIM information. Mechanical data such as ball size, thickness, and shape as well as stitch bond mechanical data were also collected. First and second bonds were subjected to destructive testing, such as ball shear and wire pull, throughout the manufacturing process.
The samples were molded using both green and non-green molding compounds. and

subjected to various industry-standard stress tests to determine the long term stability of the interface of each wire type. Data will be presented on all tests performed and will provide useful information on the material set best suited for long term reliability.

Verification of the Real-Time Wirebond Quality Control in Industrial Applications

Dott. Hesse Hesse and Knipps

As costs of field failures keep increasing in many fields of electronic applications (e.g. automotive callbacks), achievement of zero failure rates of the goods delivered to the end user becomes an imperative goal to pursue.
For ultrasonic wire bonding it is still state of the art to monitor the wire deformation and the ultrasonic current to conclude to the quality of the bonded interconnections. These signals have to show well defined time characteristics. But “Normal” wire deformation and current characteristics do not guarantee good bond quality in every case. Beside these established signals the PiQC system additionally monitors the ultrasonic frequency progression and further signals gained from a newly developed sensor integrated into the transducer. The lightweight sensor does not disturb the ultrasonic system during bonding but providing a signal very sensitive to the mechanical vibrations at the tip of the bonding tool. This sensitivity was studied and optimised by scientific analysis of the electromechanical transfer behaviour between the tool tip vibrations and the sensor signal by means of analytical and finite element models as well as corresponding measurements.
All mentioned signals are gained and processed in real-time without decelerating production speed. For each signal and derived component an individual quality index is calculated by comparison of the actual signal characteristics with reference characteristics preliminarily learned by the system in an automated procedure. Finally an overall quality index is calculated as a combination of the individual ones.
Because different types of bond failures affect the available signals in different degrees,monitoring as much as possible physically “independent” and characteristic signals provides a wide and more secure decision base for quality control.
Since several months the PiQC system is successfully applied in industrial applications at customer site. Valuable experiences could be gained in these field tests for heavy wire as well as for fine wire applications and will be discussed in this paper.